PATENT
Customer Number 22,852
Attorney Docket No. 4805.0185-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Hiroshi KOMATSU	)	Prior Application Group Art Unit: 2871
	)	
Rule 53(b) Continuation Application of	)	Prior Application
Serial No.: 09/752,441	)	Examiner: M. Ton
	)	
Filed: Herewith	)	
	)	
For: IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE	)	

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the examination of the above application, please amend this application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

Please delete the paragraph on page 6, beginning on line 1 and ending on line 13, and replace with the following new paragraph:

FIG. 2, FIG. 3a and FIG. 3b are views showing a first embodiment according to the present invention. FIG. 3a and FIG. 3b are respectively sectional views taken along line B-B' and line C-C' of the FIG. 2. As shown in these figures, gate and data bus lines

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

101 and 102 are formed on a first substrate 110, defining a pixel. Although only one pixel is drawn in these figures, a liquid crystal display device generally has a plurality of pixels. In the pixel, a common bus line 103 is formed parallel to the data bus line 101. At the cross of the gate and data bus lines 101 and 102, a thin film transistor (TFT) is formed. In the pixel, data and common electrodes 108 and 109 are disposed parallel to data bus line 102. As in the conventional IPS mode LCD, data electrode 108 has a portion overlapping common bus line 103 for obtaining a first storage capacitor (C_{s11}) as shown in FIG. 3b. In addition, common electrode 109 has a portion overlapping data electrode 108 for obtaining a second storage capacitor (C_{s12}). Common electrode 109 is connected to common bus line 103 through a hole 125.

IN THE CLAIMS:

Please cancel claim 1 without prejudice or disclaimer, and add new claims 20-50 as follows:

20. A liquid crystal display device comprising:

a first substrate;

a gate bus line and a data bus line on the first substrate;

a thin film transistor coupled to the gate and data bus lines;

a common bus line over the first substrate;

a first insulator over the common bus line;

a data electrode over the first insulator;

a second insulator over the data electrode; and

a common electrode over the second insulator.

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1300 I Street, NW
Washington, DC 20005
202.408.4000
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21. The device of claim 20, wherein the data bus line includes a highly conductive material.

22. The device of claim 20, wherein the data bus line includes one of a Mo metal layer, Mo/Al/Mo triple metal layers, or Cr/Al/Cr triple metal layers.

23. The device of claim 20, wherein the thin film transistor includes gate, source and drain electrodes.

24. The device of claim 23, wherein the gate electrode is electrically connected with the gate bus line.

25. The device of claim 23, wherein the source electrode is electrically connected with the data bus line.

26. The device of claim 23, wherein the drain electrode is electrically connected with the data electrode.

27. The device of claim 20, wherein the first insulator includes a gate insulator.

28. The device of claim 20, wherein the second insulator includes a passivation layer.

29. The device of claim 20, wherein the data electrode partially overlaps the common bus line.

30. The device of claim 20, wherein the common electrode partially overlaps the data electrode.

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HENDERSON
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1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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31. The device of claim 20, wherein the common electrode includes a transparent conductive material.

32. The device of claim 20, wherein the common electrode includes indium tin oxide.

33. The device of claim 20, wherein the common electrode is electrically connected with the common bus line.

34. The device of claim 20, wherein the common electrode is electrically connected with the common bus line through a hole in the second insulator.

35. The device of claim 20, wherein the common electrode is electrically connected with the common bus line through a hole in the first and second insulators.

36. The device of claim 20, wherein the common electrode partially overlaps the data bus line.

37. The device of claim 20, further comprising a first storage capacitor between the data electrode and the common bus line.

38. The device of claim 20, further comprising a second storage capacitor between the data electrode and the common electrode.

39. The device of claim 20, further comprising:

a first alignment layer on the first substrate.

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HENDERSON
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GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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40. The device of claim 39, wherein the first alignment layer includes one of polyimide, polyamide, polyvinylcinnamate, or polysiloxane based materials.

41. The device of claim 20, further comprising:

a second substrate;

a black matrix layer on the second substrate;

a color filter layer on the black matrix layer; and

a liquid crystal layer between the first and second substrates.

42. The device of claim 41, wherein the black matrix layer includes Cr or CrOx.

43. The device of claim 41, further comprising:

a second alignment layer on the second substrate.

44. The device of claim 43, wherein the second alignment layer includes one of polyimide, polyamide, polyvinylcinnamate, or polysiloxane based materials.

45. A liquid crystal display device comprising:

first and second substrates;

a gate bus line and a data bus line on the first substrate;

a thin film transistor coupled to the gate and data bus lines;

a common bus line over the first substrate;

a first insulator over the common bus line;

a data electrode over the first insulator;

a second insulator over the data electrode;

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HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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a common electrode over the second insulator;

a black matrix layer on the second substrate;

a color filter layer on the black matrix layer; and

a liquid crystal layer between the first and second substrates.

46. The device of claim 45, wherein the data bus line includes one of a Mo metal layer, Mo/Al/Mo triple metal layers, or Cr/Al/Cr triple metal layers.

47. The device of claim 45, wherein the common electrode includes indium tin oxide.

48. The device of claim 45, further comprising a first storage capacitor between the data electrode and the common bus line.

49. The device of claim 45, further comprising a second storage capacitor between the data electrode and the common electrode.

50. The device of claim 45, wherein the first and second alignment layers include one of polyimide, polyamide, polyvinylcinnamate, or polysiloxane based materials.

REMARKS

This application is a continuation under 37 C.F.R. § 1.53(b) of U.S. Patent Application 09/752,441 filed January 3, 2001. By this Preliminary Amendment, claim 1 has been canceled without prejudice or disclaimer of the subject matter thereof, and new claims 20-50 added.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Applicants respectfully request that the Examiner consider and allow this application.

If there are any additional fees due in connection with the filing of this Preliminary Amendment, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: January 23, 2001

By: Robert J. Rotell Reg No 24,014
for Andrew Chanho Sonu
Reg. No. 33,457

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

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APPENDIX TO PRELIMINARY AMENDMENT OF JANUARY 23, 2002

Version with Markings to Show Changes Made

Amendments to the Specification

FIG. 2, FIG. 3a and FIG. 3b are views showing a first embodiment according to the present invention. FIG. 3a and FIG. 3b are respectively sectional views taken along line B-B' and line C-C' of the FIG. 2. As shown in these figures, gate and data bus lines 101 and 102 are formed on a first substrate 110, defining a pixel. Although only one pixel is drawn in these figures, a liquid crystal display device generally has a plurality of pixels. In the pixel, a common bus line 103 is formed parallel to the data bus line [102] 101. At the cross of the gate and data bus lines 101 and 102, a thin film transistor (TFT) is formed. In the pixel, data and common electrodes 108 and 109 are disposed parallel to data bus line 102. As in the conventional IPS mode LCD, data electrode 108 has a portion overlapping common bus line 103 for obtaining a first storage capacitor (C_{s11}) as shown in FIG. 3b. In addition, common electrode 109 has a portion overlapping data electrode 108 for obtaining a second storage capacitor (C_{s12}). Common electrode 109 is connected to common bus line 103 through a hole 125.

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